23.7 A 79GHz SiGe-Bipolar Spread-Spectrum TX for Automotive Radar

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Pseudo random or pseudo noise (PN) signal processing along with direct-sequence spread-spectrum techniques has been widely used for developing powerful ranging systems [1]. These concepts are well suited also for short-range automotive radar applications in the 79GHz band. So far, VCOs and power amplifiers in SiGe technologies have been presented for the 77-to-79GHz range [2, 3]. The aim of this work is to design an integrated PN-radar transmitter containing the PN source and the biphase modulator in addition to a VCO.

Important performance characteristics of a ranging system are the supported unambiguous range d_{max} and the range resolution d_{min} (or the minimum measurable range) [1,4,5]:

$$d_{max} = \frac{1}{2}cT_p \qquad (1) \qquad\qquad d_{min} \le \frac{1}{2}cT_c \qquad (2)$$

where $T_p = NT_c$ is the period of the pseudo random sequence, N is the number of bits, T_c is the bit duration. For the system presented in this paper, N = 1023 and $T_c = \frac{1}{f_c} = \frac{1}{1.235GHz}$ have been chosen in order to achieve a d_{max} of approximately 124m and a d_{min} of less than 12cm. Considering the 79GHz carrier signal and a speed of 100km/h, the Doppler signal that can influence the correlation response of the receiver in a PN radar [5], is approximately 14.5kHz, which is much lower than the PN-code repetition frequency of 1.2MHz (it represents the spacing between the discrete lines in the spectrum of the PN signal).

The block diagram of the spread-spectrum TX chip is shown in Fig. 23.7.1. The system is fully differential and consists of four main blocks: a 79GHz VCO, a prescaler, a biphase modulator, and the pseudo-noise sequence generator. The clock signal which drives the PN source is generated on the same chip. The VCO is based on the chip presented in [2] and has a center frequency of 79GHz. The differential signal generated by the VCO drives the biphase modulator and the prescaler.

The prescaler is used to downconvert the VCO signal to 1.235GHz. It consists of six divider stages. The first stage is a dynamic divider which is faster than a static divider while consuming less power. The dynamic divider is also preferred for the injection-locked divider since it does not limit the tuning range of the system. An injection-locked divider can show a better input sensitivity around the frequency of interest in this application, but its operating range is very narrow compared to that of a dynamic divider. The other five stages are static dividers optimized for low power consumption. Since the signal from the prescaler has to drive all the clocked stages in the PN generator, a buffer has been connected at the output of the last divider stage.

The PN sequence is generated by a pseudo random bit sequence (PRBS) generator. The PRBS generator consists of a clock input stage, a linear feedback shift register (LFSR) [1,6], and an output buffer. Three cascaded emitter followers are used in the clock input stage in order to shift down the DC level of the clock signal and drive the LFSR. The shift register contains n=10 stages and generates a maximum-length sequence of N=2^n–1 = 1023b. Each stage is a delay element which has been implemented as a flip-flop. The performance of the overall system at 79GHz strongly depends on the quality of the baseband PN signal and it is quite challenging to integrate baseband together with high-speed blocks. Recently, new techniques have been presented to improve the performance of flip-flops connected in a divider configuration [7,8]. Such techniques are based on asymmetric current levels in the reading and holding path in each latch. This asymmetry leads to a longer reading time against a shorter holding time which makes the flip-flop faster. In order to improve the shape of the output signal from the PRBS, in our design the concept of asymmetry has been used, but in the opposite way. As shown in Fig. 23.7.2, in each latch a resistor has been placed in the reading path to unbalance the tail current I_o in the holding path. In this way, the holding time will be longer than the reading time. Because of this asymmetry, spikes in the output signals are avoided during clock transitions, as shown in Fig. 23.7.3. In the third stage another differential pair has been also implemented to force the initial condition in the LFSR. In order to achieve a fast switching behaviour at the upper differential pairs of the modulator, an output buffer has been integrated in the PRBS to achieve a maximum differential output swing of $1.4V_{pp}$.

The biphase modulator shifts the baseband spectrum of the PRBS to the carrier frequency. The fully differential biphase modulator is implemented as a Gilbert cell and shown in Fig. 23.7.4. The lower differential pair of the modulator is driven by the 79GHz carrier and the upper pairs by the PN signal. Since the bit rate of the PN signal is very low compared to the frequency of the carrier, the modulator works mostly as a cascode thereby improving its performance. Transmission lines are used as load in the modulator and also for on-chip matching.

The measurements are performed on wafer at room temperature. The baseband output from the PRBS is connected to a spectrum analyzer. The RF-modulated signal is connected via a W-band waveguide to a W-band downconversion mixer, which downconverts the 79GHz modulated signal to an IF of 4.646GHz. This output is applied to a second spectrum analyzer. The measurement results are shown in Figs. 23.7.5 and 23.7.6. The very good shape of the baseband signal validates the technique used in the design of the LFSR. Its quality also determines the precise shape of the upconverted signal, which shows that there is only a small feedtrough of the carrier. The slight asymmetry in the measured spectrum shape of the upconverted signal is due to the variation of the conversion loss of the downconversion mixer at different IF frequencies. The spectral nulls at Δf =±1.235GHz can clearly be seen in the baseband and upconverted signal spectra. The measured differential output power from the modulator is –1dBm (the 2.5dB insertion loss of the probe has not been taken into account), which is good enough for short-range applications without an additional PA stage.

The complete integrated system draws 750mA from a 5.5V supply. The chip is manufactured in an advanced SiGe:C 200GHz f_T bipolar process based on the technology presented in [9]. A die micrograph is shown in Fig. 23.7.7. The size of the IC is 1128×1028µm^2.

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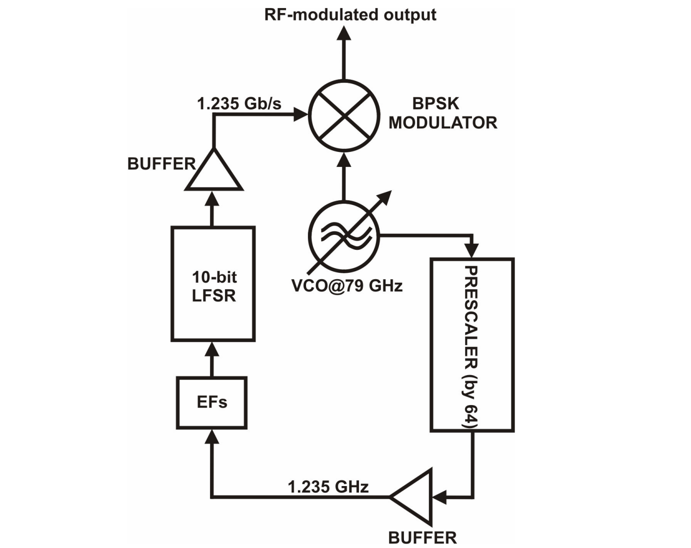

Figure 23.7.1: Block diagram of the transmitter.

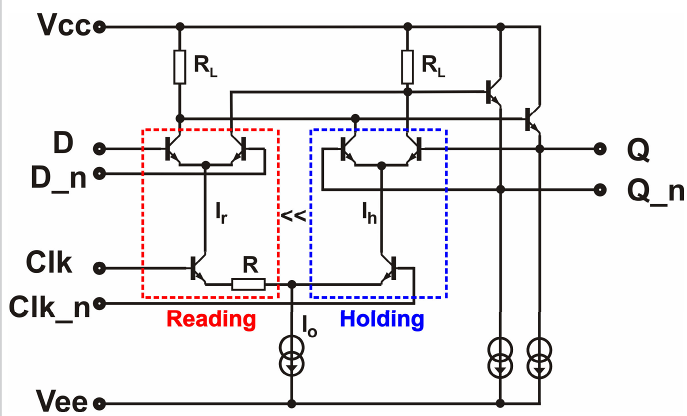

Figure 23.7.2: Latch schematic: introduction of a resistor in the reading path, $I_r << I_h$.

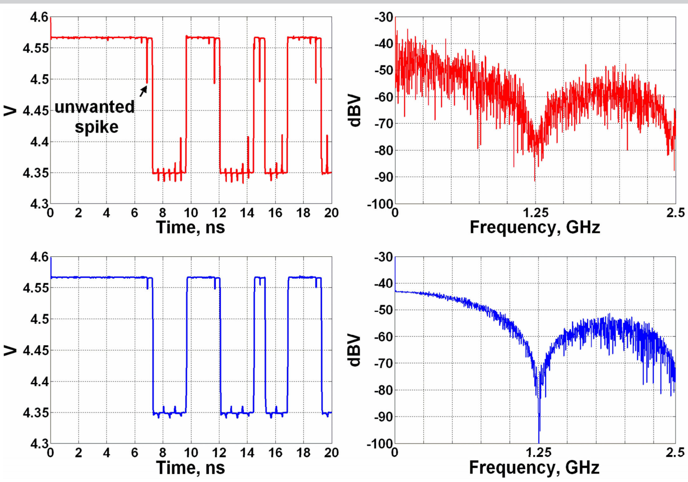

Figure 23.7.3: Simulation results of a PRBS. Effect on the spectrum of the unwanted spikes in the time domain response (upper figures). Attenuation of the spikes by using a resistor in the reading path of each latch results in a better shape of the PN signal in the frequency domain (lower figures).

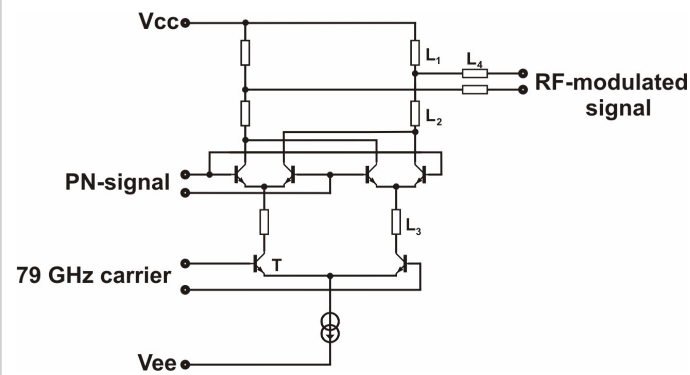

Figure 23.7.4: BPSK-modulator schematic. L_1, L_2, L_3, and L_4 are microstrip-line elements, all with inductive behaviour.

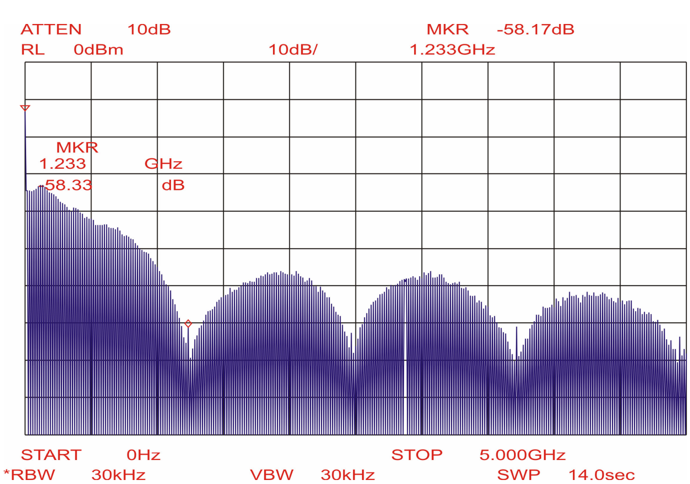

Figure 23.7.5: PN baseband signal spectrum.

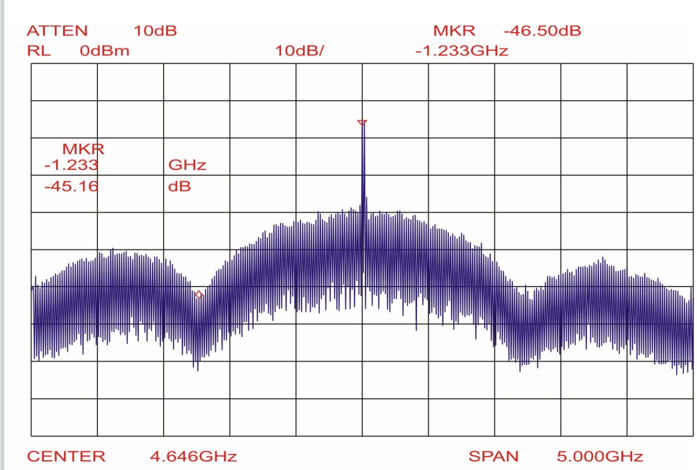

Figure 23.7.6: RF-modulated signal spectrum downconverted to an intermediate frequency of 4.646GHz.

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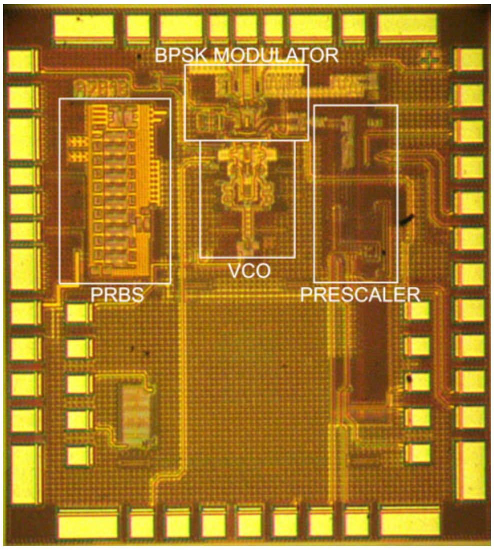

Figure 23.7.7: Chip micrograph.

